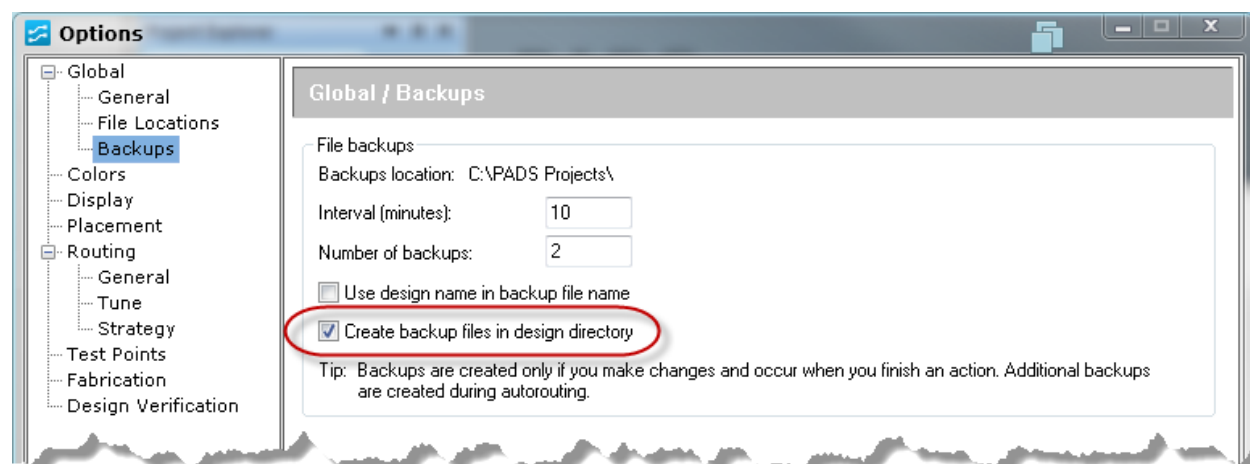
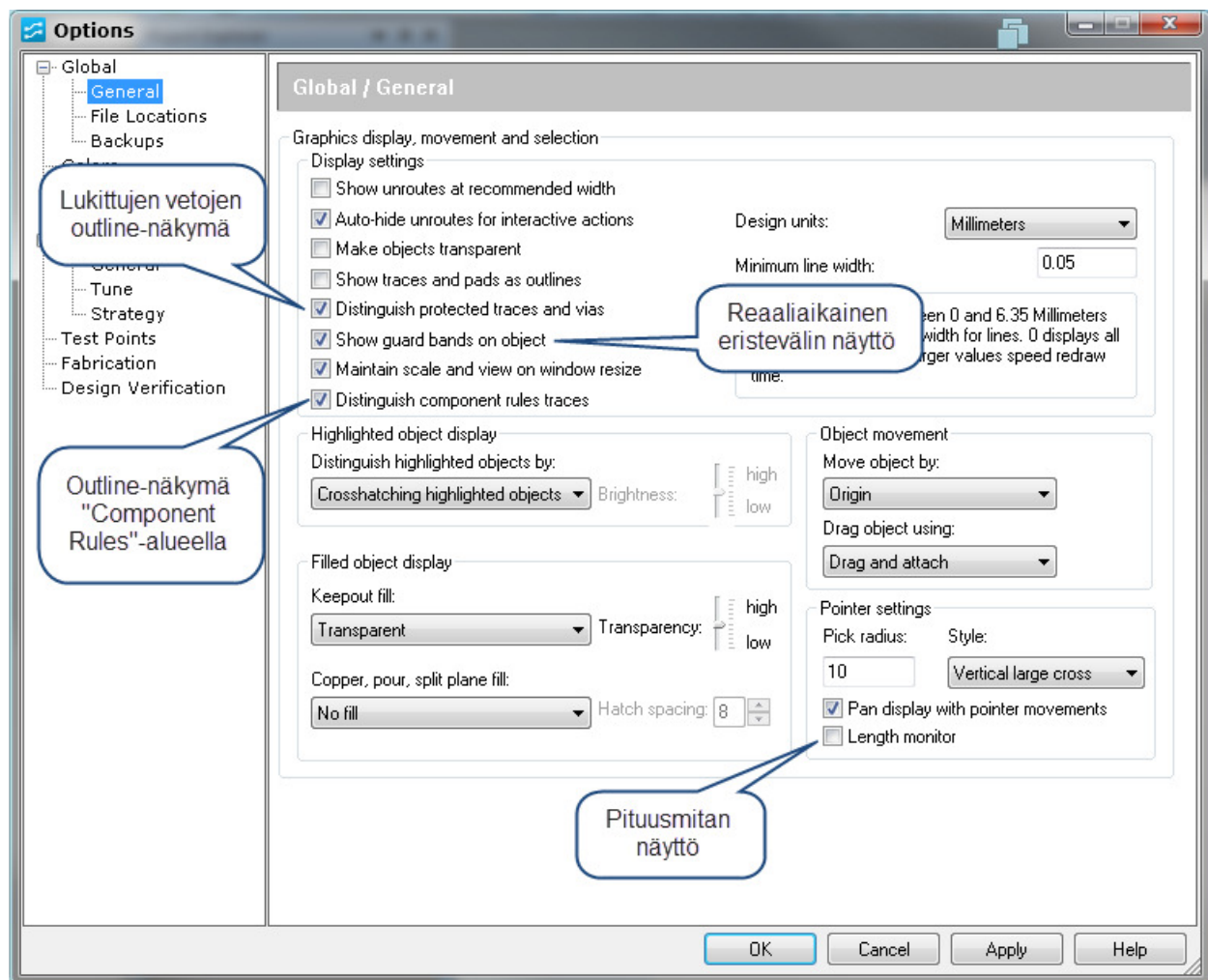
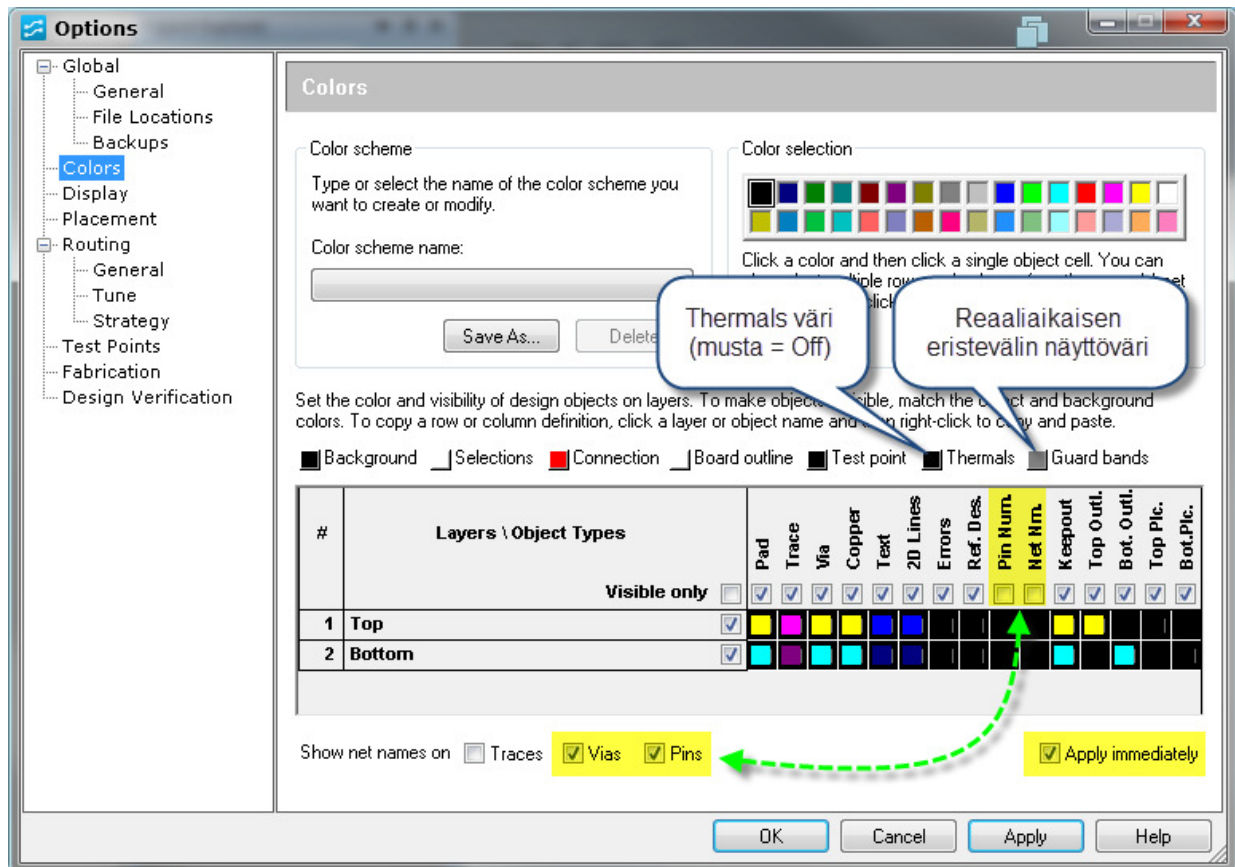


PADS VX Router perusasetukset

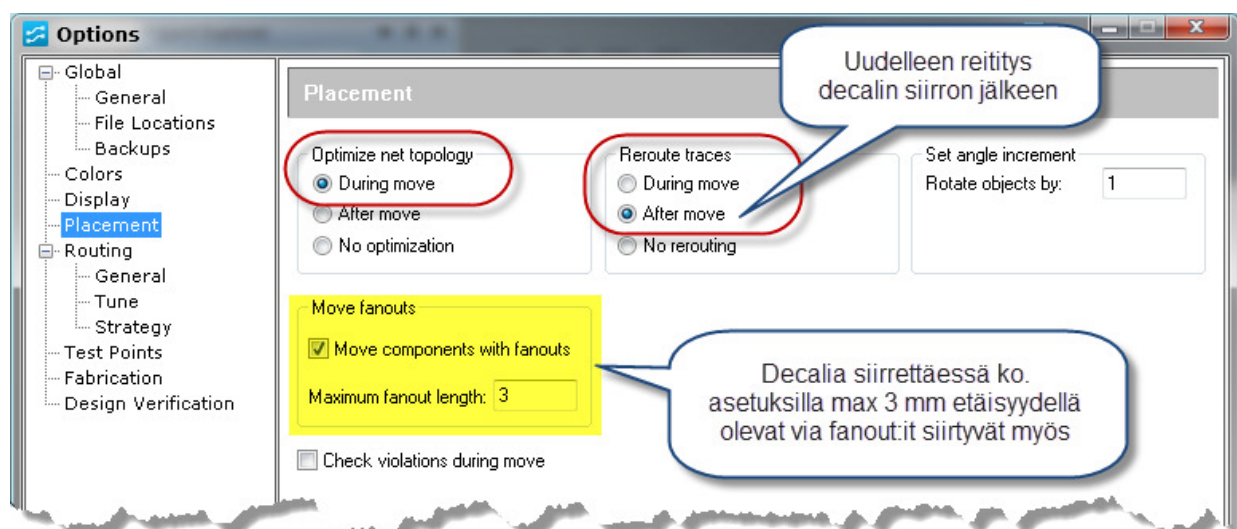
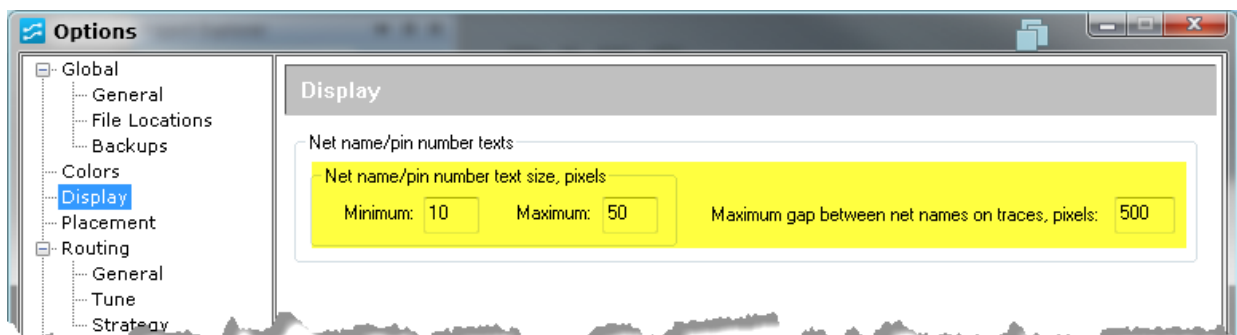
Seuraavat asetukset ovat hyvät perusasetukset PADS Router-ohjelman käyttöönottoa varten, joilla Interaktiivisuus menee myös maksimiin.

Options:

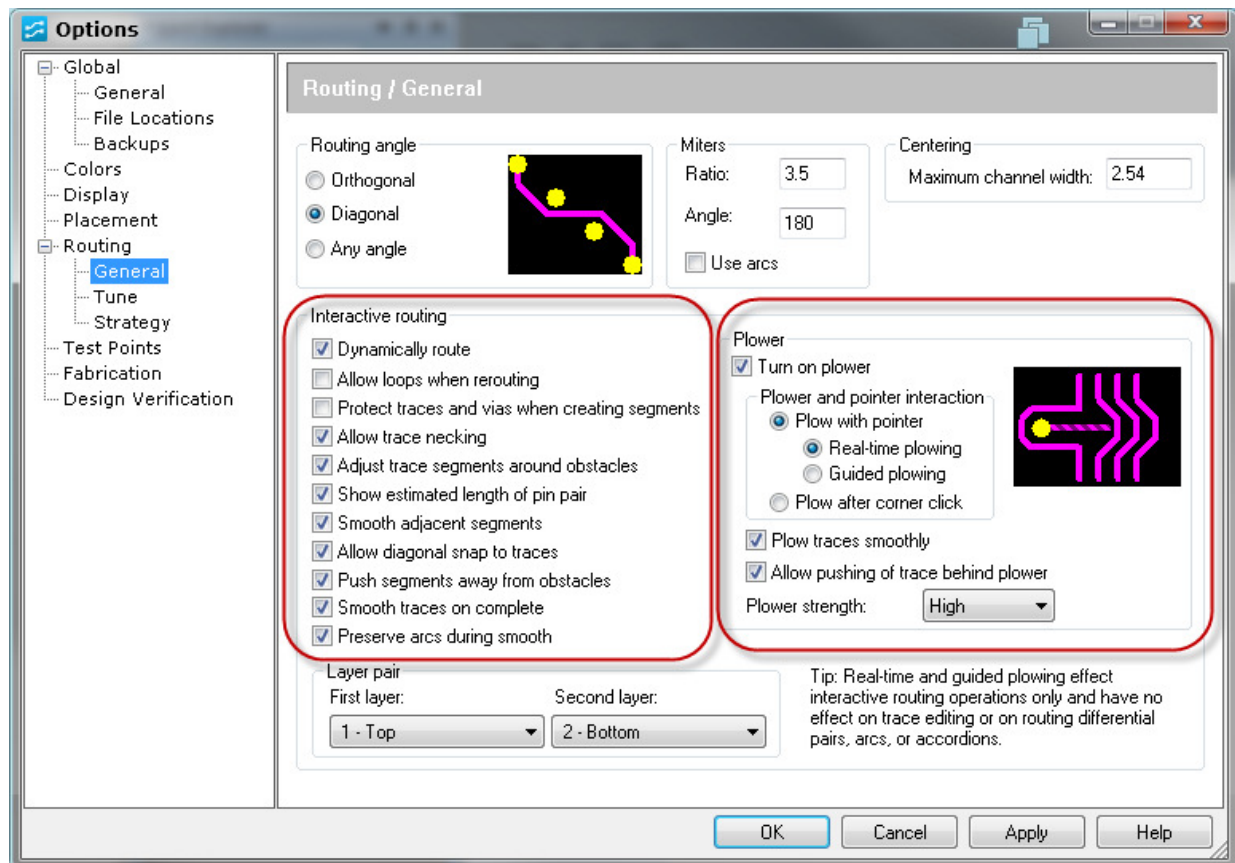




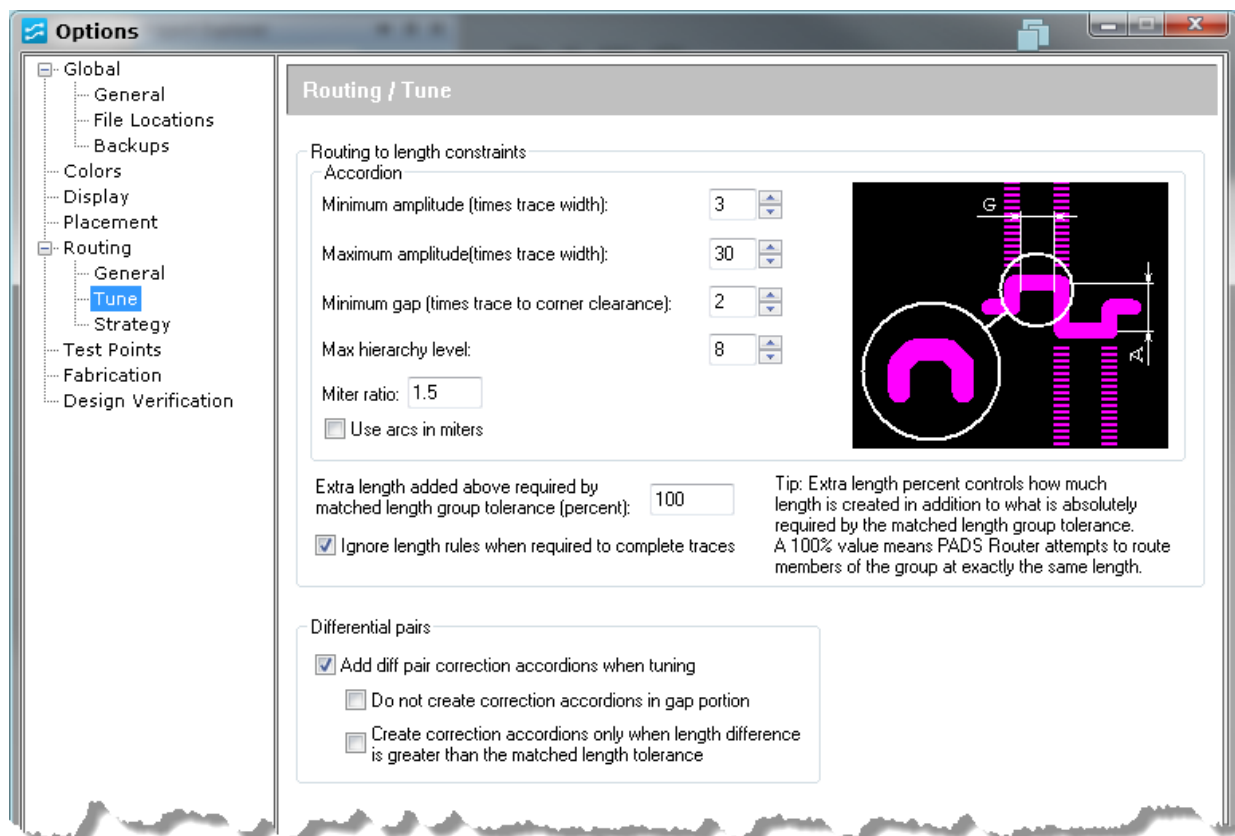
"Net Name" koko ja toisto-määrittäminen, jos "Traces" valittu "Show net names on"-kohdassa:



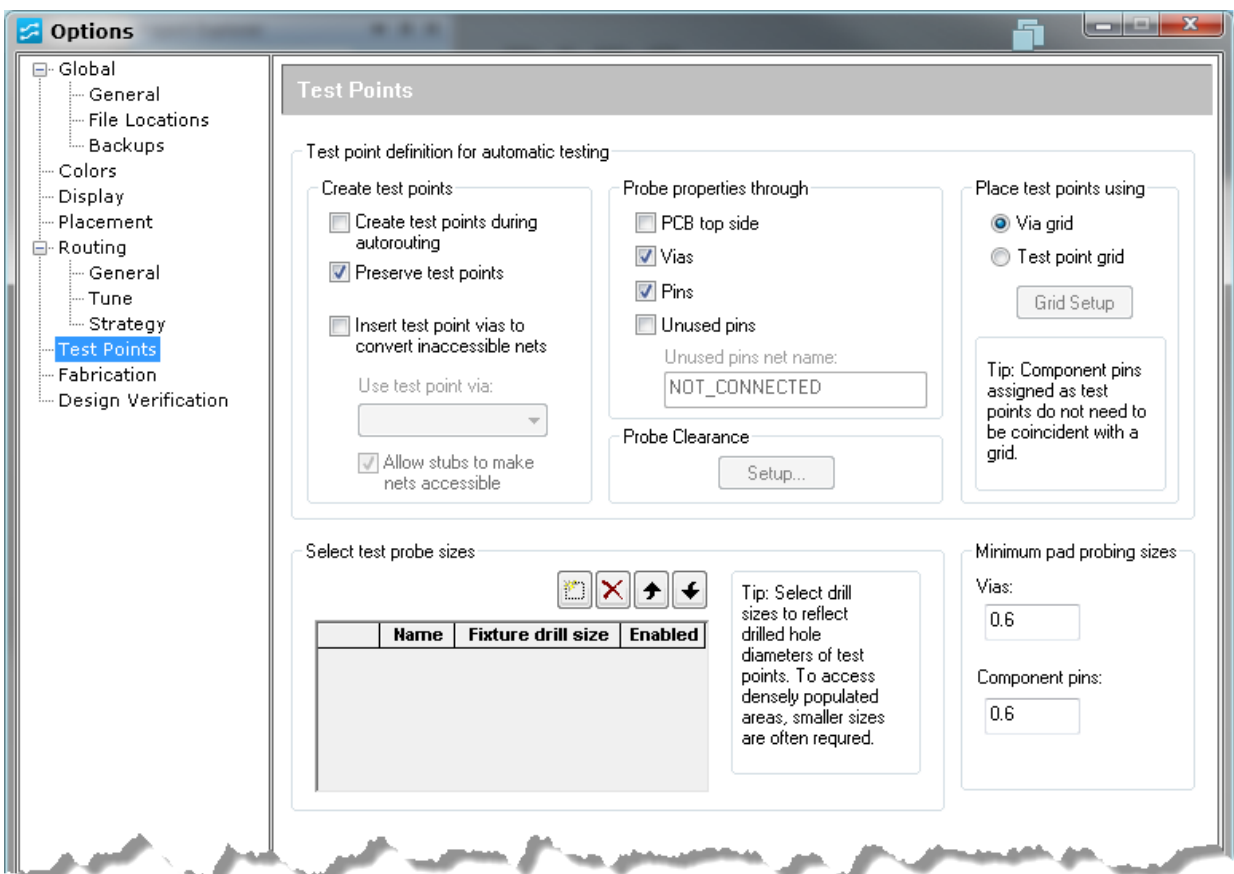
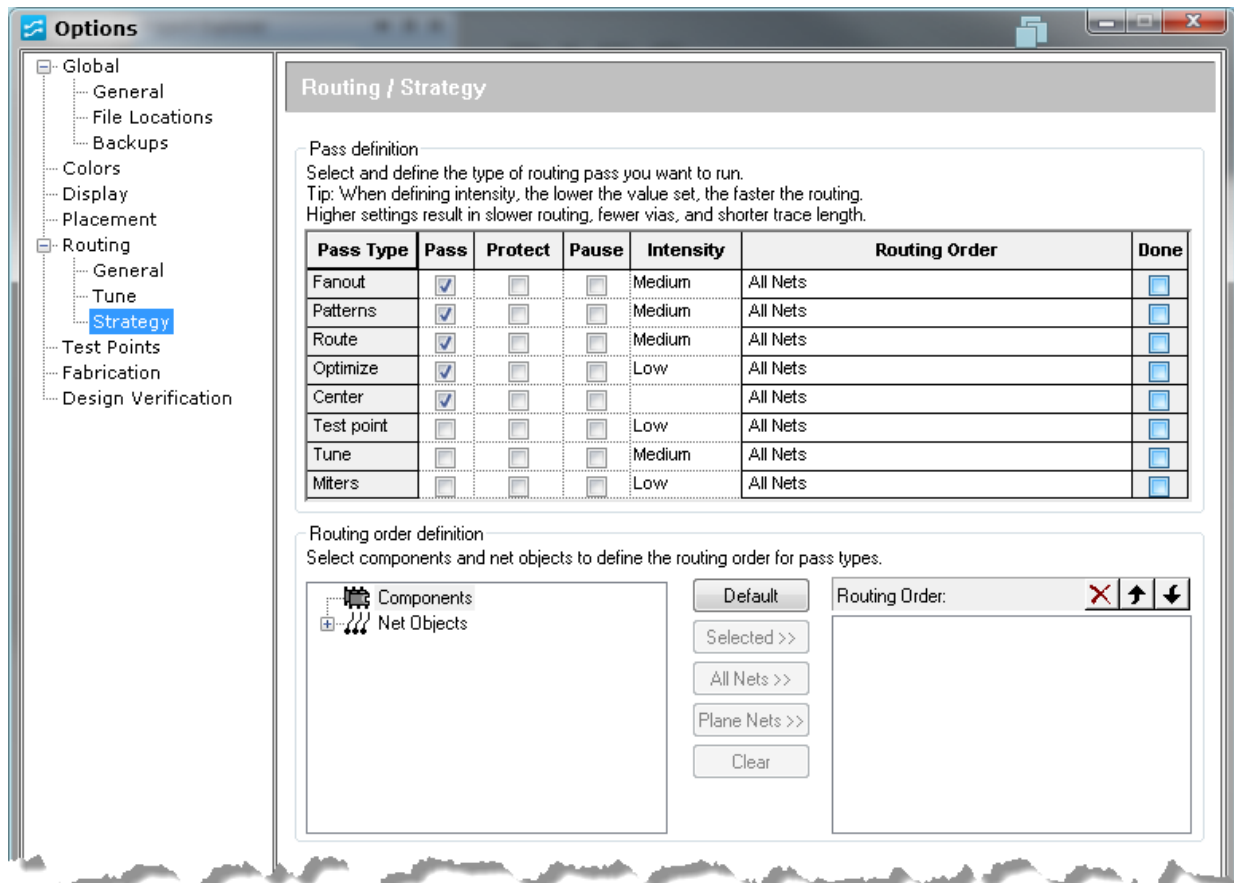
"Interactive routing" ja "Plower" asetukset vaikuttavat Routerin toimintaan, kun reititetään käsin. Oheisilla asetuksilla interaktiivisuus on asetettu maksimiin.

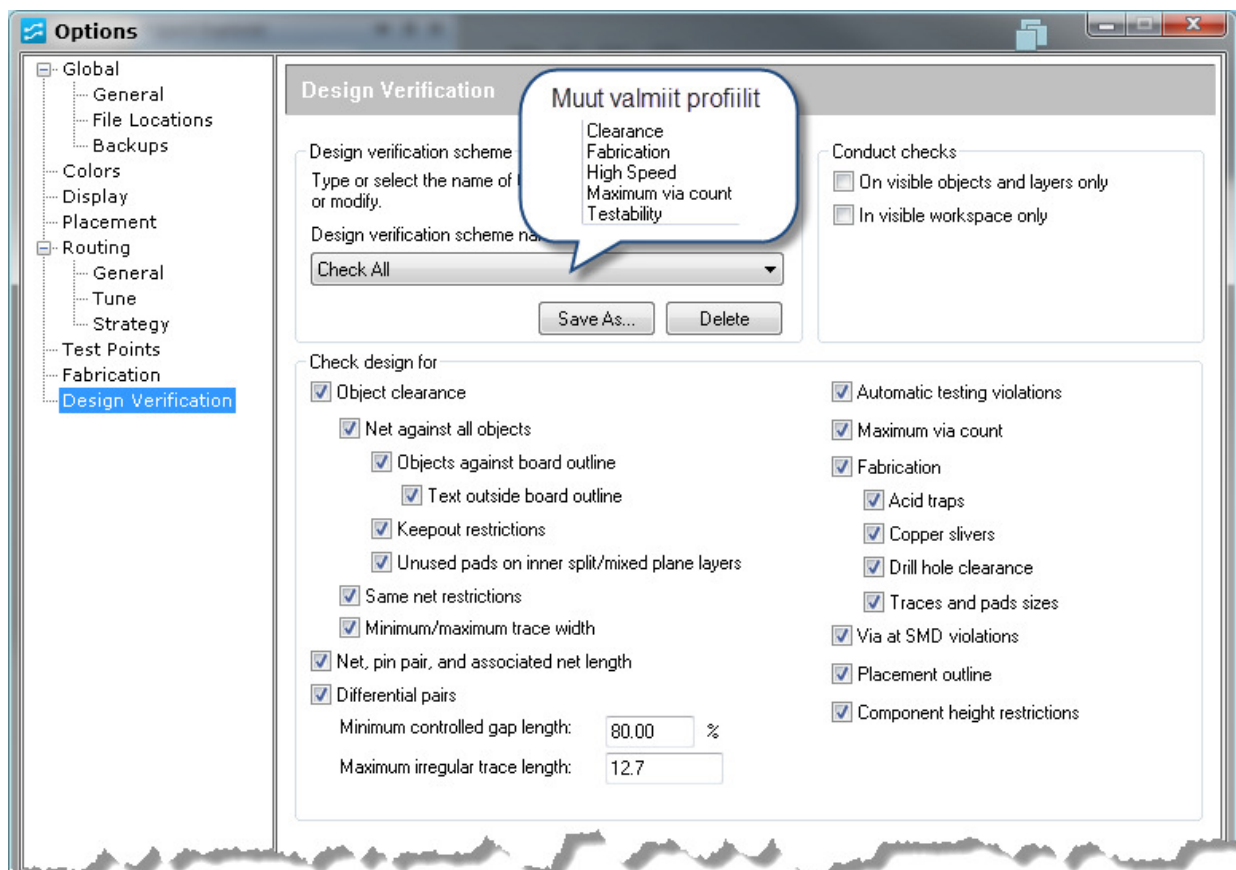
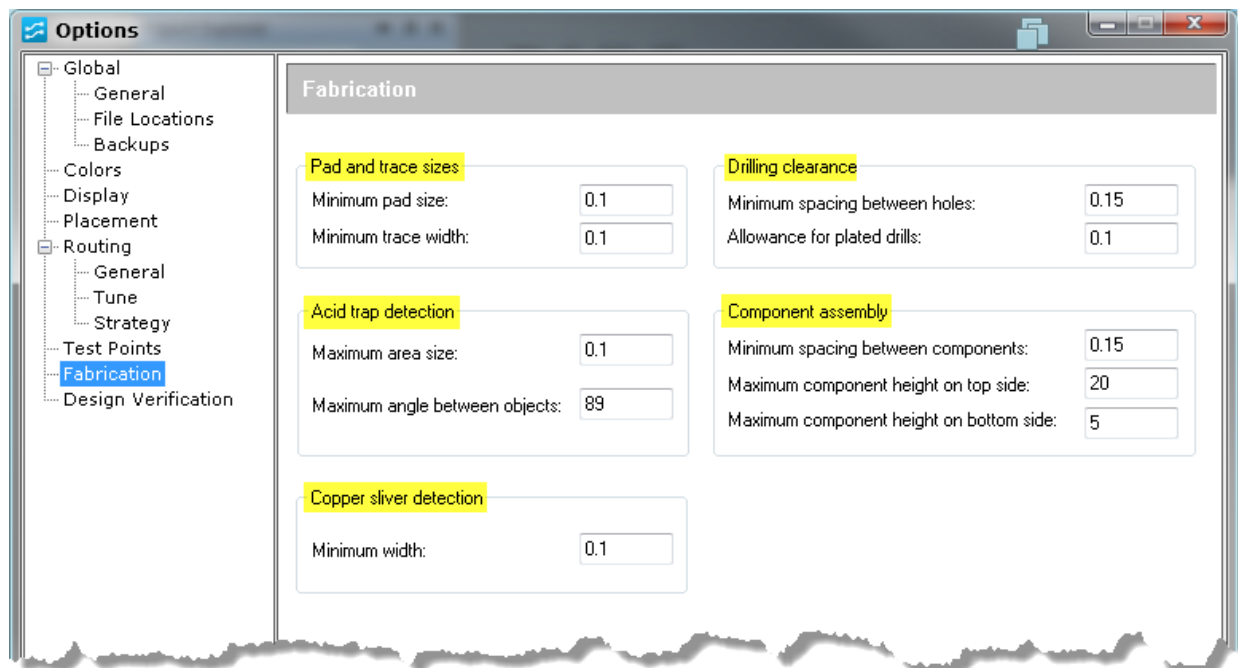


Pituusmitoitettujen vetojen "Tune" säännöt.



AutoRouterin asetukset.





Design Properties:

Lukuarvot oheisissa asetuksissa esimerkkiarvoja, mitkä kannattaa asettaa suunniteltavan työn vaativuuden ja piirilevyvalmistajan mahdollisuuksien mukaan.

Design Properties

Test Points	Layers	Grid	Fanout	Pad Entry	Topology
Clearance	Routing	Via Biasing	Layer Biasing	Same net	

To set the minimum allowable clearance between an object listed in the left column and those in the other spreadsheet columns, enter a number between 0 and 25.4 Millimeters within the cell for each object type. Click a row or column header to set the same value for all objects in that row or column. Click All to set the same value between all design objects listed.

All	Trace	Via	Pad	SMD	Text	Copper	Board	Drill
Trace	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
Via		0.1	0.1	0.1	0.1	0.1	0.1	0.1
Pad			0.1	0.1	0.1	0.1	0.1	0.1
SMD				0.1	0.1	0.1	0.1	0.1
Copper						0.1	0.1	0.1

Test Points	Layers	Grid	Fanout	Pad Entry	Topology
Clearance	Routing	Via Biasing	Layer Biasing	Same net	

Trace width

Minimum:	Recommended:	Maximum:
0.1	0.15	0.2

Tip: The trace must have a minimum width equal to or less than the width of each pad it enters during routing.

Maximum number of vias

☒ Unlimited vias
 ☐ Maximum of: 60

Tip: The maximum number of vias only applies to autorouting

Routing

☒ Allow autorouting
 ☒ Allow trace unrouting

☒ Shove traces to complete connection when required

☐ Shove protected traces when required

Test Points	Layers	Grid	Fanout	Pad Entry	Topology
Clearance	Routing	Via Biasing	Layer Biasing	Same net	

Specify whether to allow vias if needed with

Via	Allow	Type	First Layer	Last
B2-5	☒	Partial	Inner Routing Layer 2	Inner Routing Layer 5
L1-2	☒	Partial	Component Side Layer 1	Inner Routing Layer 2
L5-6	☒	Partial	Inner Routing Layer 5	Solder Side Layer 6
STANDARDVIA	☒	Thru	Component Side Layer 1	Solder Side Layer 6
TESTPOINT	☐	Thru	Component Side Layer 1	Solder Side Layer 6
VDDVIA	☐	Thru	Component Side Layer 1	Solder Side Layer 6

Käytettävissä olevat läpiviennit

Test Points	Layers	Grid	Fanout	Pad Entry	Topology
Clearance	Routing	Via Biasing	Layer Biasing	Same net	

Specify whether to allow routing on a layer when routing. If you want to allow routing on a layer, click the Layers tab.

Layer	Allow Routing
Component Side Layer 1	☒
Inner Routing Layer 2	☒
Gnd Plane Layer 3	☐
VDD Mixed Plane Layer 4	☐
Inner Routing Layer 5	☒
Solder Side Layer 6	☒

Preview

Sallitut reitityskerrokset

Test Points	Layers	Grid	Fanout	Pad Entry	Topology
Clearance	Routing	Via Biasing	Layer Biasing	Same net	

Object clearance

To set the minimum allowable clearance between an object listed in the left column and those in the other spreadsheet columns, enter a number between 0 and 25.4 Millimeters within the cell for each object type. Click a row or column header to set the same value for all objects in that row or column. Click All to set the same value between all design objects listed.

All	Via	SMD	Trace	Pad
Corner	0.1	0	0.1	
Via	0.1	0.1		

Eristevalisäännöt saman netin sisällä

Clearance	Routing	Via Biasing	Layer Biasing	Same net
Test Points	Layers	Grid	Fanout	Pad Entry

Object clearance

To set the minimum clearance between a probe and those objects specified in the other spreadsheet columns, enter a number between 0 and 25.4 Millimeters within the cell for each object type. Click a row or column header to set the same value for all objects in that row or column. Click All to set the same value between all design objects listed.

All	Probe	Trace	Pad	Body	Board
Probe	0.35	0.15	0.15	0	3

Maximum length of trace stubs: 3.5

Clearance
Routing
Via Biasing
Layer Biasing
Same net
Test Points
Layers
Grid
Fanout
Pad Entry
Topology

Set the routing direction and effort level (cost) used to complete routing when autorouting layers.
Tip: When defining layer cost, specify a value between 0 and 100. Setting values greater than 0 will reduce the usage of the layer during autoroute operations.

Autorouterin reititys-suunnat

Routing parameters for layers

	Layer	Route	Direction	Type	Cost
1	Component Side Layer 1	☒	Horizontal	No plane	0
2	Inner Routing Layer 2	☒	Vertical	No plane	0
3	Gnd Plane Layer 3	☐	Vertical	Split/Mixed	0
4	VDD Mixed Plane Layer 4	☒	Horizontal	Split/Mixed	0
5	Inner Routing Layer 5	☒	Horizontal	No plane	0
6	Solder Side Layer 6	☒	Vertical	No plane	0

Preview

Clearance
Routing
Via Biasing
Layer Biasing
Same net
Test Points
Layers
Grid
Fanout
Pad Entry
Topology

Interaktiivinen Router toimii parhaiten kun Routing ja Via "Snap Objects to Grid" eivät ole aktiivina

Grid Type	X Increment	Y Increment	Snap Objects to Grid
Displayed	0.127	0.127	
Routing	0.05	0.05	☐
Test Point	1.27	1.27	☒
Via	0.1	0.1	☐
Fanout	0.2	0.2	☐
Component	0.1	0.1	☒

Clearance
Routing
Via Biasing
Layer Biasing
Same net
Test Points
Layers
Grid
Fanout
Pad Entry
Topology

Create fanouts
For pins on ☒ Plane nets
☒ Signal nets
☐ Unused nets

Allow multiple connection to
☒ Pin ☒ SMD ☒ Via ☒ Trace

Fanout length
☒ Unlimited Maximum: 6.35

Placement of via fanout for:
SOIC / QUAD BGA BGA staggered

Alignment: Alternate, multiple Direction: Both sides Spacing: Use grid

Preview

Clearance
Routing
Via Biasing
Layer Biasing
Same net
Test Points
Layers
Grid
Fanout
Pad Entry
Topology

Pad Entry
Enter pads through
☒ Side ☒ Corner ☐ Any angle

☒ Ignore first corner rules to complete traces when required

Preview

Via at SMD placement
☒ Allow vias on surface mount pad

☒ Fit inside ☒ Center ☐ Ends

Preview

Clearance
Routing
Via Biasing
Layer Biasing
Same net
Test Points
Layers
Grid
Fanout
Pad Entry
Topology

Net topology type
☐ Protected ☒ Minimized ☐ Serial ☐ Parallel ☐ Mid-driven

Preview

Allow junctions on
☒ Vias ☒ Traces

Maximum stub length: 0

Tip: To disable T-junctions, clear the Traces check box.